ISSN No.: 2454- 2024 (online)

International Journal of Technical Research & Science

Design and Implementation of Digital Components Using Reversible Logic Gates

Ravi JN, Dr. Vijay Prakash AM, Madan S
Email id: ravijn095@gmail.com
Department of ECE, Bangalore Institute of technology, Bangalore

Abstract- Implementing the already existing circuits using reversible logic has drawn a significant interest in recent years as a promising computing technique having application in low power CMOS, quantum computing, nanotechnology, optical computing, etc. Reversible logic gates offer significant advantages such as high speed, low power, ease of fabrication …etc. Also, circuits designed using these circuits would have better performance as compared to existing circuits. Main goals of reversible logic synthesis is to minimize the garbage, to minimize the delay, to minimize the total number of gates and also to minimize the width of the circuit. In this paper, designer implemented 2:1 MUX, D-Flip-Flop and PIPO shift register using reversible logic gates.

1. INTRODUCTION

Basic concepts required to understand the reversible logic gates are described below.

1.1 Why Reversible Logic Gates?

When a computational system erases a bit of information, it must dissipate (kTln2) Joules of energy, where, 'k' is the Boltzmann's constant and 'T' is the temperature which has been proved experimentally. For T=300k (room temperature), this is about 2.9X10^-21 Joules [1]. This is roughly the kinetic energy of a single air molecule at room temperature. Today's computers will erase a bit of information, every time they perform a logic operation. These logic operations are therefore called "Irreversible". This erasure is done very efficiently and much more than (kT) Joules of energy is dissipated for each bit erased. If we are to continue the revolution in computer hardware performance, we must continue to reduce energy dissipated by each logic operation. It can be reduced, by improving conventional methods, i.e., by improving the efficiency by reducing the power dissipated.

An alternative approach is to use logic operations that do not erase information. These are called "Reversible logic" operations and in practical applications they can dissipate arbitrarily less heat. As the energy dissipated per irreversible logic operation approaches the fundamental limit of (kTln2) Joules, the use of reversible operations is likely to become more attractive. Hence, if we wanted to reduce energy dissipation per logic operation, below (kTln2) Joules, we will be forced to use reversible logic.

1.2 Basic Reversible Logic Gates

There are different types of reversible logic circuits are available. In this paper, author have used two of them, namely – Feynman gate (FG) and Toffoli gate (TG). Boolean expression s for each of those two gates are shown in block diagrams below, at each output pins.

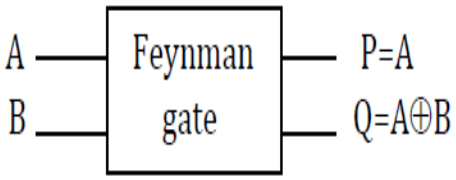


Fig. 1.1 Basic Block diagram of FG gate

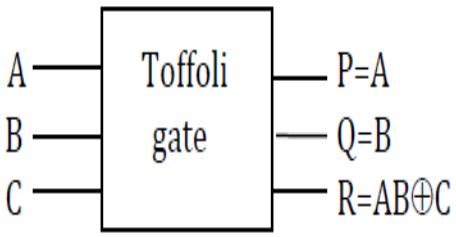


Fig. 1.2 Basic Block diagram of TG gate

2. PROPOSED DESIGN METHODOLOGY

Different logic circuit can be realized by using reversible logic gates. This paper presents a better way to build a circuit which requires less power for its operation, lesser delay time…etc. Some of the design approaches for different logic circuits with reversible logic gates are below.

2.1 Design and Implementation of D FLIP FLOP Using Reversible Logic Gates

In a D flip flop, there are two inputs and two outputs pins are present. Basically, it can be constructed with the help of basic gates. Design of d flip flop using NAND gates is shown in figure 3.

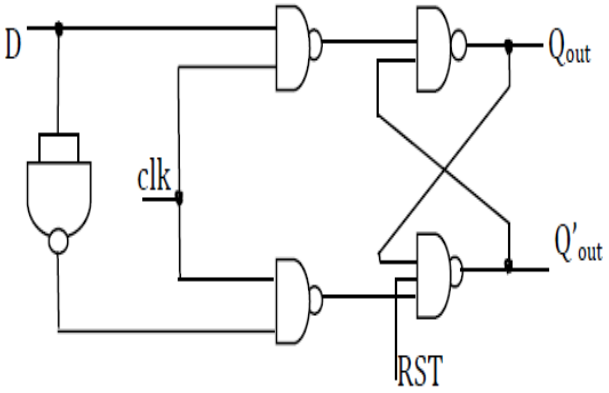


Fig. 2.1 Basic circuit diagram of D-flip flop

Table-2.1 Truth table for D flip flop

Inputs				Output
RST	clk	D	Q_n (past ouput)	$Q_{n+1}=Q_{out}$ (present output)
0	×	×	×	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

It is also known as a 'Data' or 'Delay' flip flop. The d flip flop captures the value of d input at a definite portion of the clock cycle (here rising edge of the clock). Truth table in table 1 of a D-Flip-Flop. From the above truth table characteristic equation of D Flip Flop can be written as,

$$Q_{n+1}=RST\ [D.\ CLk + \overline{CLK}.Q_n]$$

When enable signal Clk(Clock) is 1, the value of input 'D' is reflected at output, i.e, $\mathbf{Q_{n+1}=D}$. While, when Clk=0, it maintains its previous state, i.e, $\mathbf{Q_{n+1}=Q_n}$.. Reversible D flip flop using Feynman and Toffoli gates is shown in figure 8. Here 'RST' is a active low type reset signal. Figure shows the realization of reversible D-flip flop using Feynman and Toffoli gates. There are 10 garbage output pins are present i.e, those 10 pins are not required for D flip flop operation. They are used just to satisfy the basic criteria of reversible logic gate, i.e. number inputs should be equal to number of outputs.

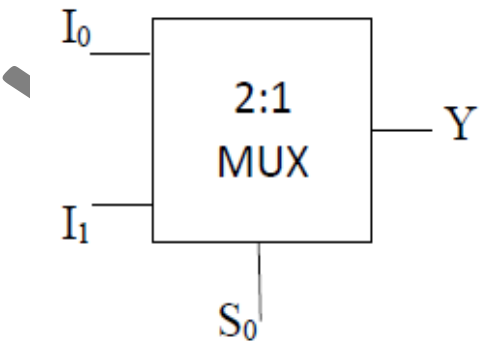
2.2 2:1 MUX realization using Reversible logic gates

A 2:1 MUX (multiplexer) is a combinational circuit with 2 inputs (I_0 & I_1) and 1 output (Y). Particular input will appear at the output (Y), depending on the status of a pin, called 'Select Line' (S_0), as shown in truth table. Boolean equation of 2:1 MUX, using the below truth table will be,

$$Y=\overline{S}_0\, I_0 + S_0\, I_1$$

Block diagram for 2:1 mux is shown in fig. 2.2 along with its truth table in Table-2.2. Also, fig. 2.3 shows the block diagram representation of reversible 2:1 mux.

Table-2.2 Truth Table for 2:1 mux



Select Line	Output
S_0	Y
0	I_0
1	I_1

Fig. 2.2 Block Diagram for 2:1 Mux

Here, S_0 be the select line input & I_0, I_1 be the input lines and 'Y' be the output pin. This expression can be used to realize 2:1mux. Figure4 shows, the block diagram for the realization of 2:1 mux using reversible logic gate. Here, designer constructed the circuit for 2:1 Mux using Feynman and Toffoli gate.

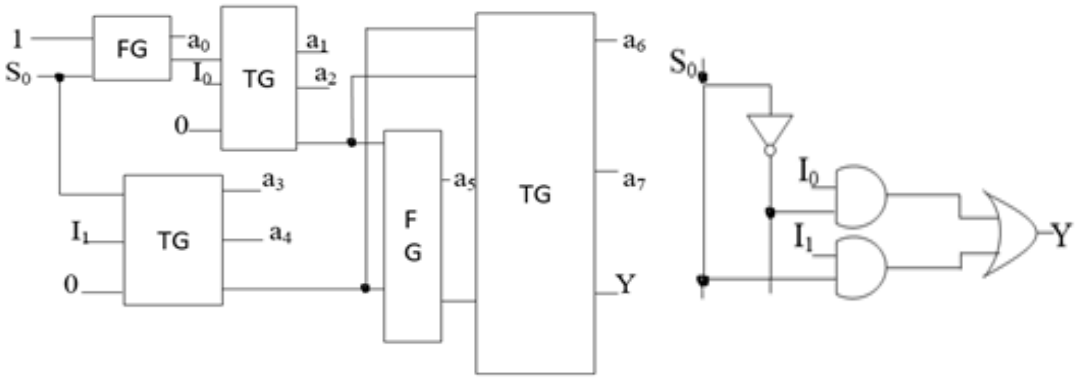


Fig. 2.3 Block diagram for 2:1 Mux using reversible gates **Fig. 2.4 Circuit Diagram for 2:1 mux**

2.3 Design of PIPO Circuit Using D flip flop

Pipo (parallel input parallel output) is a type of operation under which shift register can be used. Shift registers are a type sequential logic circuit, mainly used for storage of digital data. They contain a group of flip flops connected in a chain, so that the output from one flip flop drives the other one. All are driven by a common clock and all are setted or resetted simultaneously.

Basic types of shift registers are:

- Serial In-Serial out (SISO)
- Parallel in Serial out (PISO)
- Parallel in Parallel out (PIPO)
- Serial in-Parallel out(SIPO)

In this paper, designer implemented the PIPO shift registers operation. Fig. 2.6, shows block diagram for the realization of PIPO circuit using 4, D Flip Flops (reversible) with 4 inputs and 4 output lines. Each D Flip Flop is constructed by considering the conceptual design approach used in (2.1) section in this paper.

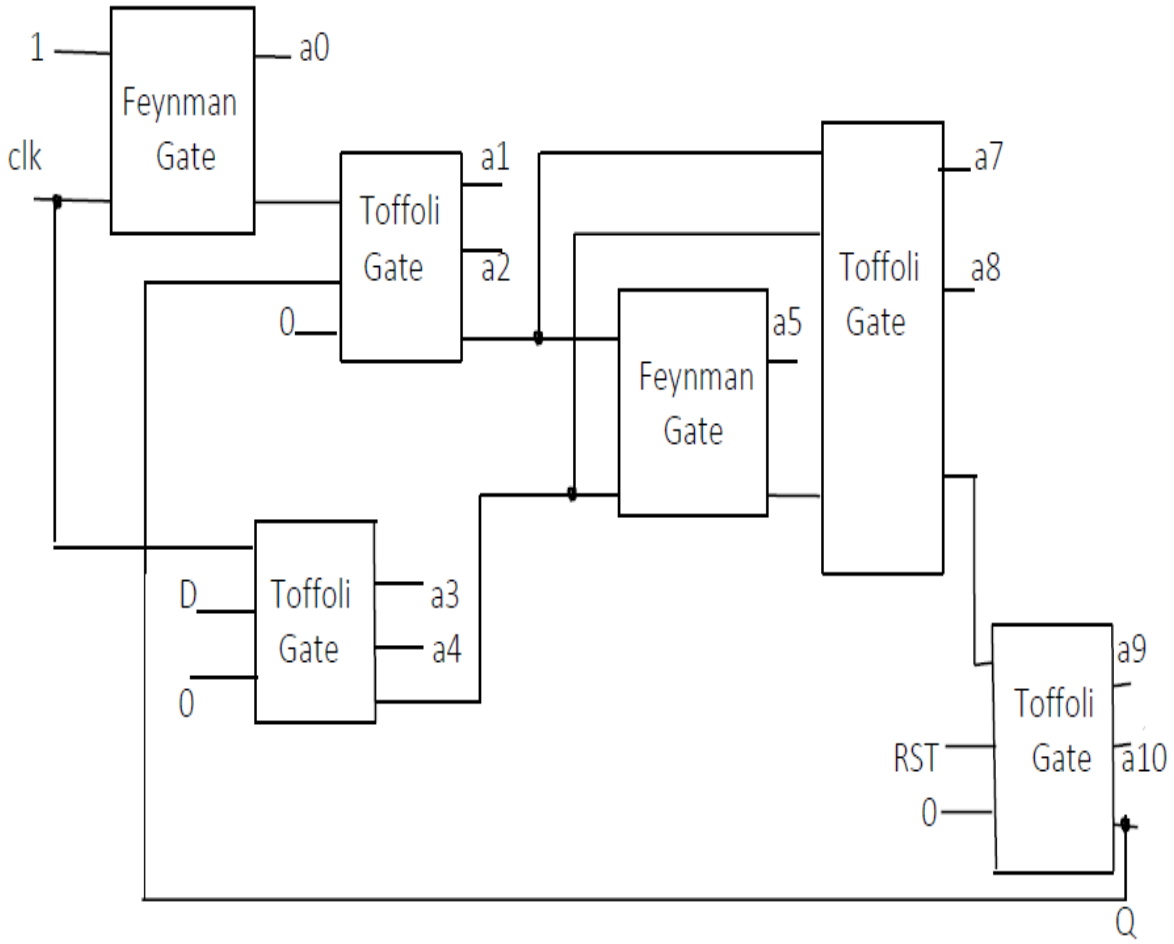


Fig. 2.5 Block diagram of D flip flop

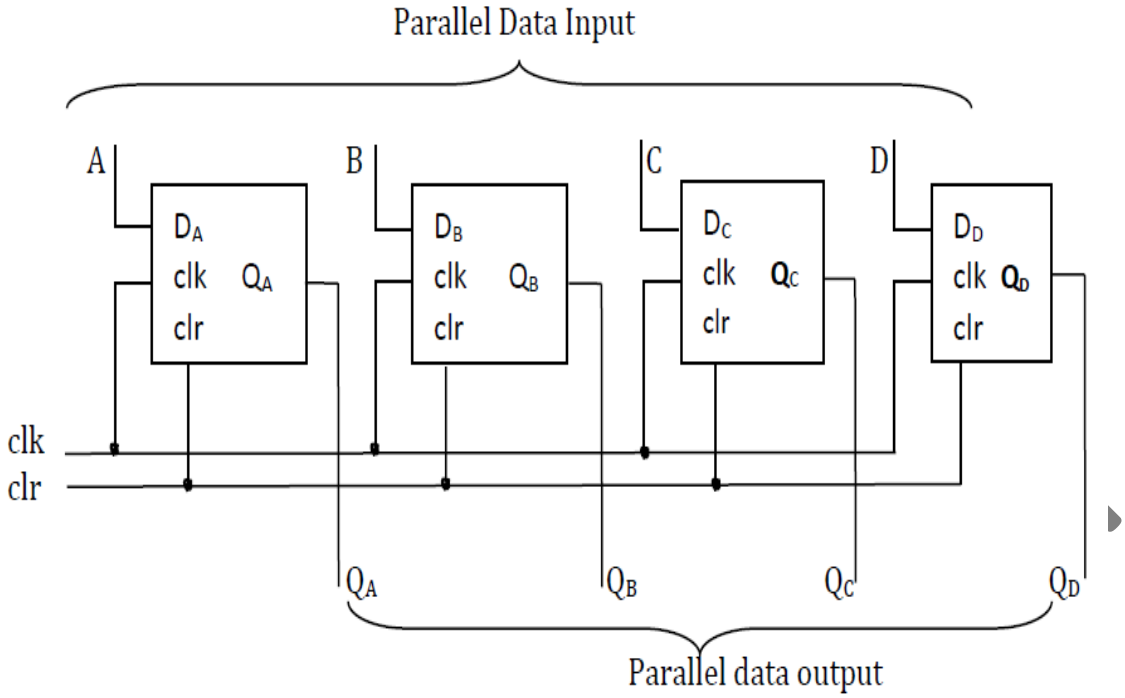


Fig. 2.6 Block diagram of PIPO circuit

RESULTS & CONCLUSION

Simulation Results

This section deals with the simulation results which are obtained for each circuits. The proposed circuits are simulated on Modelism tool and synthesized for Xilinx Spartan-3 with Device 3s4000fg676-5. For all the above mentioned circuits i.e, for d-flip flop, pipo & 2:1 mux functionality is verified by using Xilinx ISE 9.1i software. Results can be easily verified with the help of waveforms for each case. Simulated snapshot input, output waveforms of the proposed circuits are shown from figure 10 to figure 12.

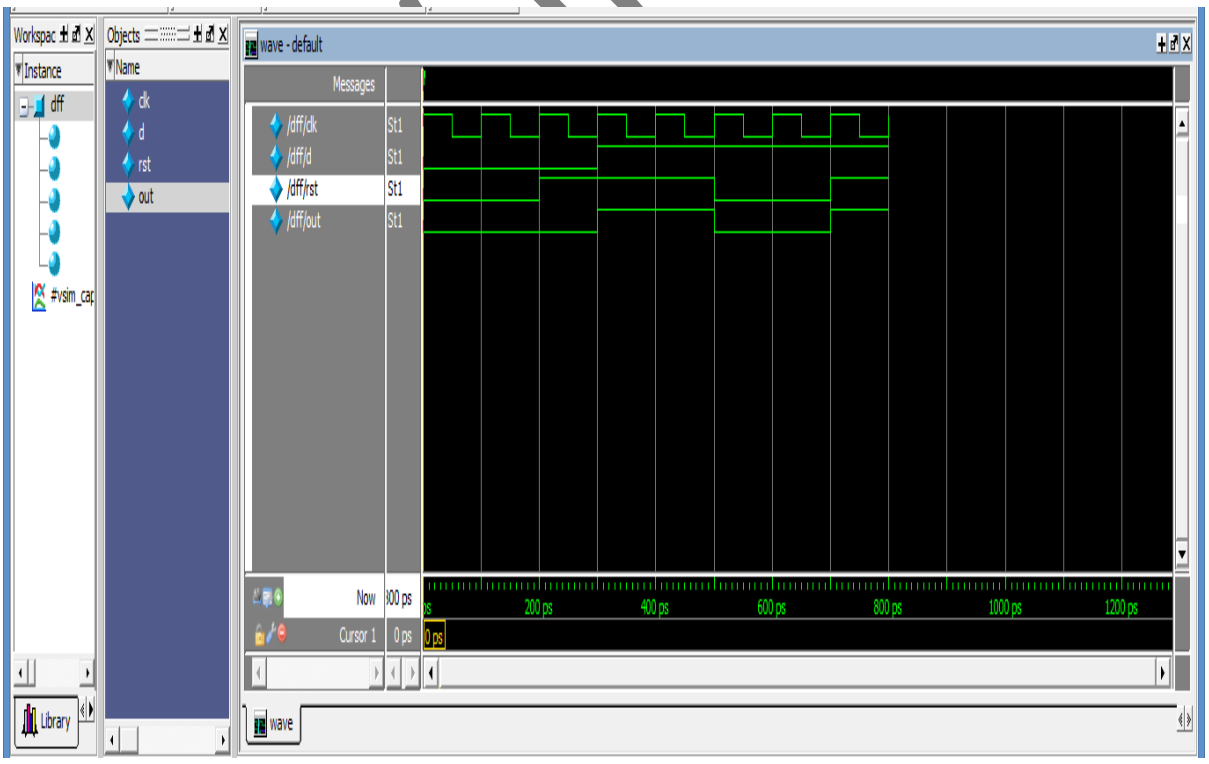


Fig. (A) Simulation Result for D flip flop

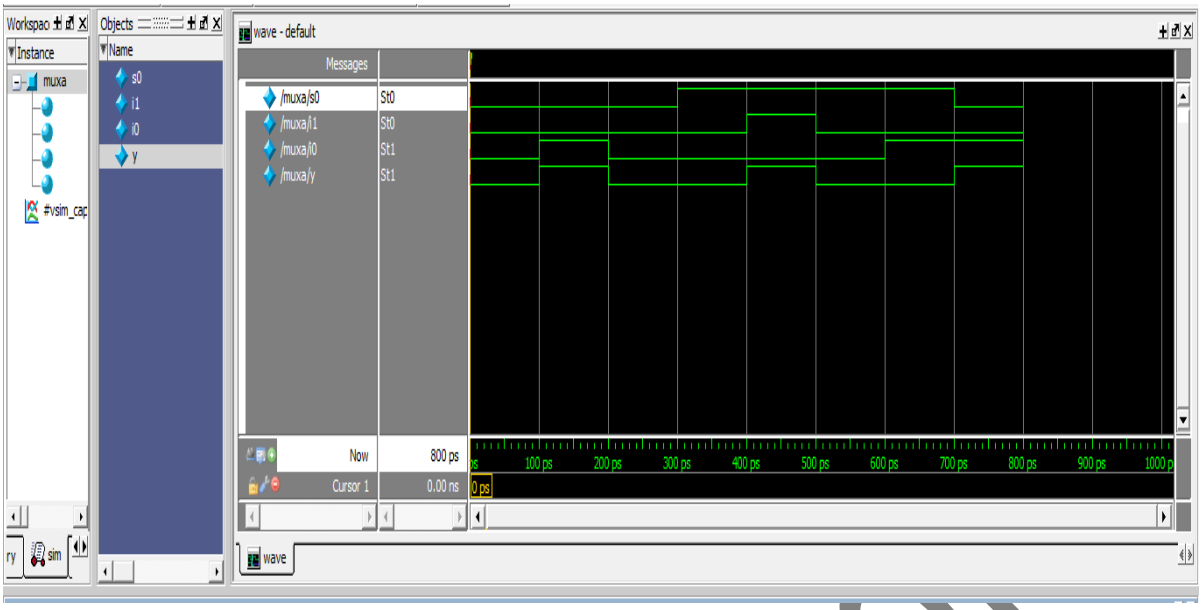


Fig. (B) Simulation result for 2:1 mux

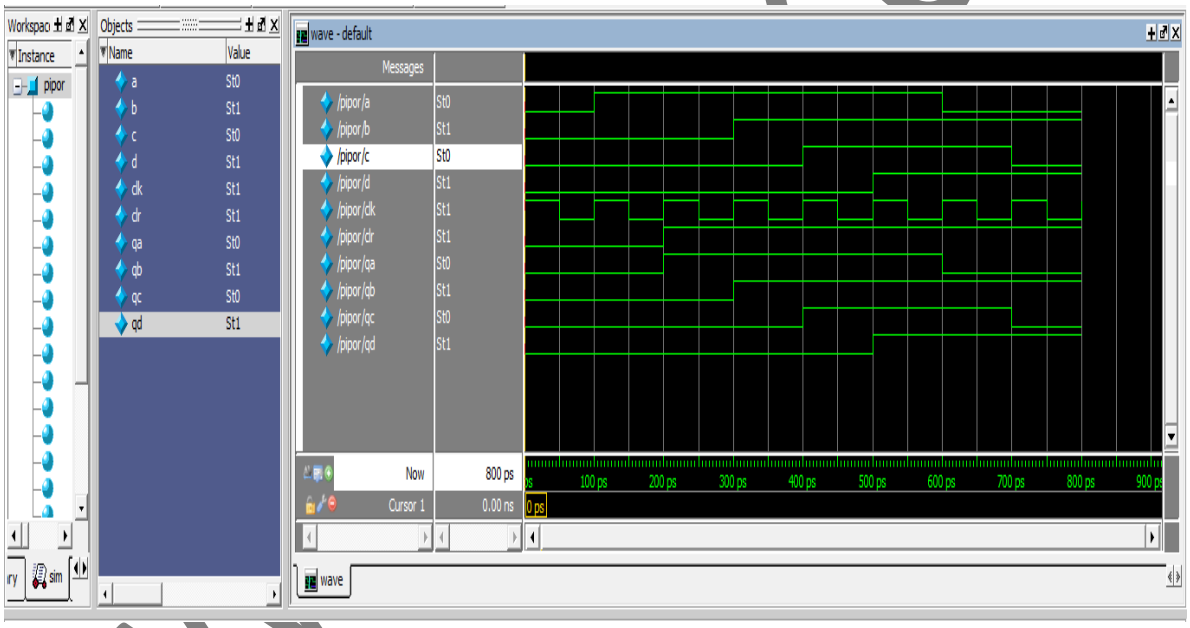


Fig. (C) Simulation Result for PIPO Shift Register

SYNTHESIS RESULTS

Synthesis results for the above designed circuits are shown below in terms of delay generated out that circuit and power consumption by that circuit.. Simulation results for 3 gates discussed in this paper is shown below with the help of timing diagram. D flip flop, 2:1 mux, pipo circuits are tested for its functional correctness and the results are simulated by using Xilinx software. In this paper, D flip flop is implemented along with Reset facility. That reset facility is not available in the circuits designed in the papers which are included as a reference to this paper.

Table-A Delay & Power Consumption of Designed Circuits

Reversible circuits	Delay (ns)	Power (mw)
D flip flop	7.824	257
Pipo	7.923	257
2:1 mux	7.760	56

Table-B Device Utilization Summary for D flip flop

Selected Device	3s4000fg676-5(Spartan 3)
Number of Slices	1 out of 27648 0%
Number of 4 input LUTs	1 out of 55296 0%
Number of IOs	4
Number of bonded IOBs	4 out of 489 0%

Table-C Device Utilization Summary for PIPO

Selected Device	3s4000fg676-5(Spartan 3)
Number of Slices	2 out of 27648 0%
Number of 4 input LUTs	4 out of 55296 0%
Number of IOs	10
Number of bonded IOBs	10 out of 489 2%

Table-D Device Utilization Summary for 2:1 MUX

Selected Device	3s4000fg676-5(Spartan 3)
Number of Slices	1 out of 27648 0%
Number of 4 input LUTs	1 out of 55296 0%
Number of IOs	4
Number of bonded IOBs	4 out of 489 0%

CONCLUSION

In this paper, author discussed about D flip-flop, pipo shift register and 2:1 mux in terms of their respective power consumption. Power consumption, delay generated and device utilization summaries for each of above mentioned circuits are shown in table 10. It has been seen that power consumption can reduced in the implementation of any logic circuit using reversible logic gate, as mentioned in the introduction part (in section 1.1). Here, author simulated and synthesized the logic circuits using Xilinx software. Also, author implemented them by using Feynman and Toffoli gates, but other reversible gates can also be used for this purpose. Proposed circuits have applications in digital circuits like reversible processor, quantum computing, etc…

REFERENCES

[1] Prashanth R Yelekar, Prof. Sujata, S Chiwande, "Introduction to Reversible Logic Gates and its Application", NCICT, 2011.

[2] Nagarjun S, Nagendra R, Kiran N KIran Kumar K N, "Design and comparison of Reversible and irreversible sequential logic circuits", ISSN (online):2347-2812, Volume-2, Issue-4, 2014

[3] B.Raghu kanth, B.murali Krishna, M. Sirdhar, V.G. Santhi Swaroop, "a distinguish between reversible & conventional logic gates", IJERA, Vol-2, Issue 2, Mar -Apr 2012, pp .148-151

[4] Shefali Mamataj, DibyaSaha, Nahida Banu ,"A review of reversible gates & its application in logic design",AJER,Vol-03,Issue-04, pp-151-161

[5] Himanshu Thapliyal and Nagarajan Ranganathan, "Design of Reversible Sequential Circuits Optimizing Quantum Cost, Delay, and Garbage Outputs", ACM Journal on Emerging Technologies in Computer Systems, Vol.6, No. , Article14, Published date: December2010.

[6] Mr. Devendra Goyal and Ms. Vidhi Sharma, "VHDL Implementation of Reversible Logic Gates", IJATER, ISSN NO: 2250-3536 , VOLUME 2, ISSUE 3, may 2012

[7] FatemeNaderpour, AbbasVafaei, "Reversible Multipliers: Decreasing the Depth of the Circuit", ICECE 2008, 20-22 December 2008, Dhaka, Bangladesh.